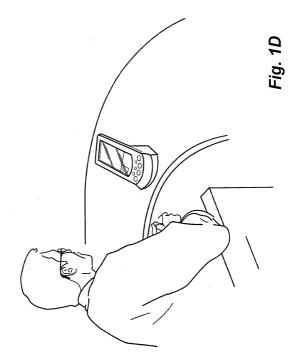
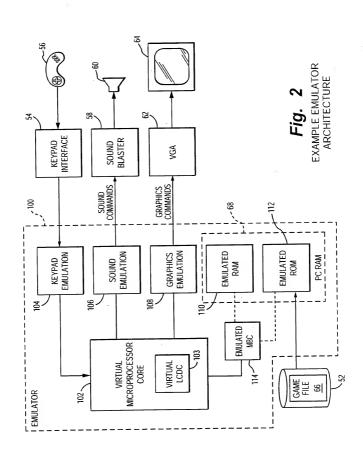


Fig. 1B

Fig. 1C





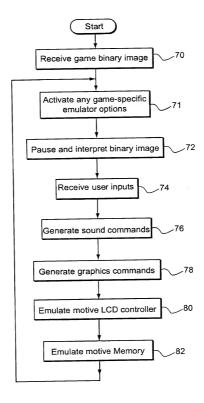


Fig. 2A

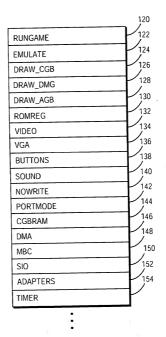
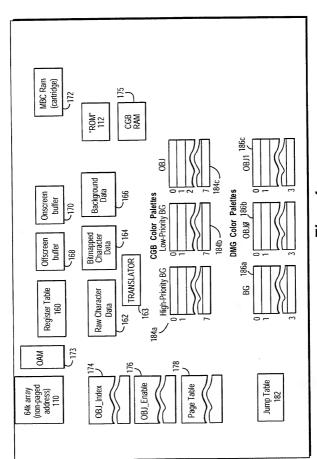
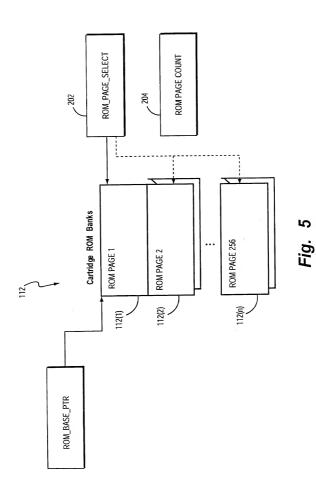


Fig. 3 EXAMPLE FUNCTIONAL MODULES



**Fig. 4** EXAMPLE MEMORY OBJECTS



EXAMPLE EMULATED CARTRIDGE ROM

Fig. 6

## Compatibility modes:

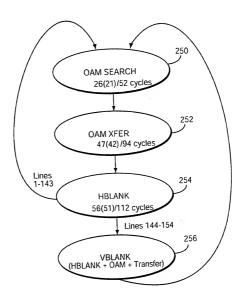
CGB_INCOMPATIBLE
CGB_COMPATIBLE
CGB_EXCLUSIVE
AGB

## Registration Data Locations:

ROMREG_CGB	
ROMREG_CARTRIDGE	
ROMREG_ROM	
ROMREG_RAM	

Fig. 7

Fig. 8
EXAMPLE VIRTUAL LCD CONTROLLER STATE MACHINE



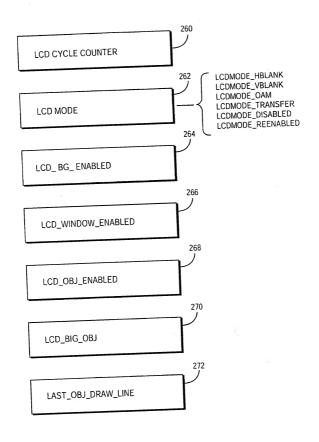
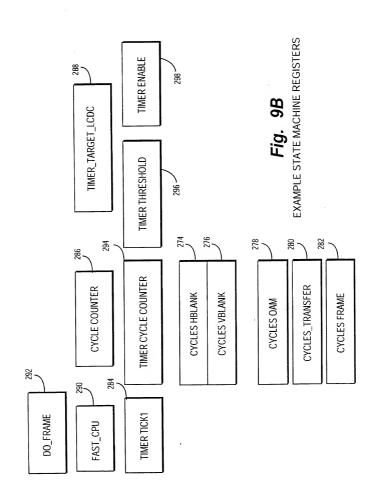


Fig. 9A

EXAMPLE LCD CONTROLLER EMULATION



Cycles per Event	DMG	CGB
HBLANK	56 (51)	112
OAM SEARCH	26 (21)	52
OAM TRANSFER	47 (42)	94
VBLANK	(HBLANK + OAM + TRANSFER)	(HBLANK + OAM + TRANSFER - 30)
FRAME	(VBLANK * 154)	(VBLANK * 154)

Fig. 9C EXAMPLE STATE MACHINE CYCLE PARAMETERS

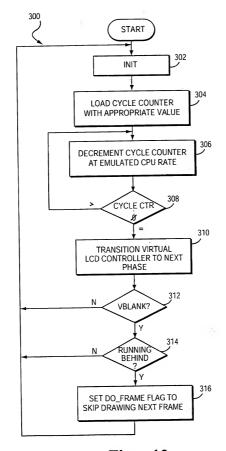


Fig. 10
EXAMPLE LIQUID CRYSTAL DISPLAY CONTROLLER

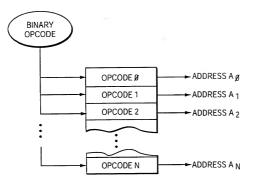


Fig. 11
EXAMPLE OPCODE JUMP TABLE

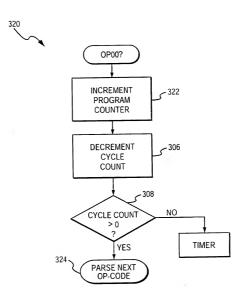
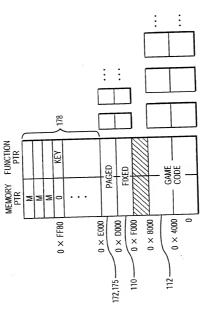


Fig. 12
EXAMPLE NOP EMULATION



**Fig. 13** EXAMPLE PAGE TABLE

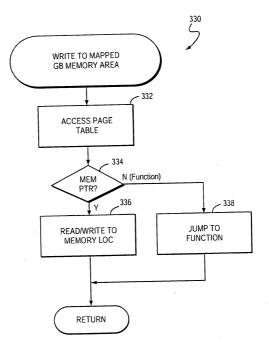


Fig. 14
EXAMPLE MEMORY ACCESS OPERATION

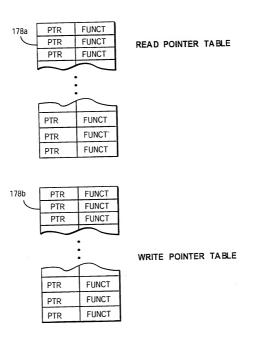


Fig. 15
EXAMPLE READ + WRITE TABLES

TOR	0x01	0x02	0x04	0x10	0x08		ENABLE FLAG		U FLAGS:					Fig. 16	EXAMPLE	REGISTER EMULATION	
	INTERRUPT_VBLANK	INTERRUPT_LCDC	INTERRUPT_TIMER	INTERRUPT_BUTTONS	INTERRUPT_SIO		354 INTERRUPT MASTER ENABLE FLAG	2	STER A GAMEBOY CPU FLAGS:	354a CARRY FLAG	354b HALF-CARRY FLAG	354c ADD SUB FLAG	354d ZERO FLAG	Example Microprocessor	352 VIIIdal Registers Faure		
REGISTERS	(BC)	(DE)	Ę	<u> </u>	(FA)	(SP)	7		Z80 LONG REGISTER	pc	əb	모	af	ds	Ψ.	STICK_PTR	1
Z80 R	cphh	edhh	-		afhh	hhhds			Z80 F	- (	2005					STICK	
7356	cph	edp		E I	afh	sphh			358	$\mathcal{T}$					350		 
REGISTERS:	q	-	, .	٩	4	yds			Z80 WORD REGISTERS:	pch	deh	恒	afh	yds	۳ <u>ر</u> ا	PROGRAM_PTR	
Z80 BYTE REGISTERS:	J		د	_	в	lds	-		Z80 WORD	pc	de	모	af	g.		PRO	
1								_									_

•

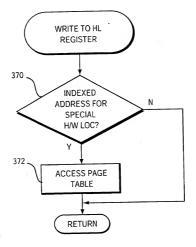
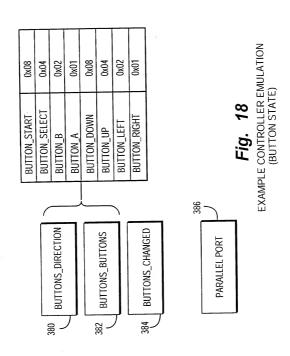


Fig. 17
EXAMPLE HL REGISTER
WRITE OPTIMIZATION



## GAME SPE CIFIC E MULATION OPTIO NS:

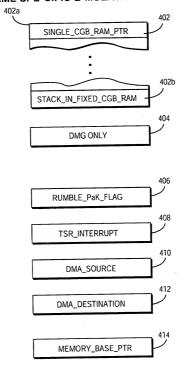


Fig. 19A

EXAMPLE VIRTUAL MICROPROCESSOR DATA STRUCTURES

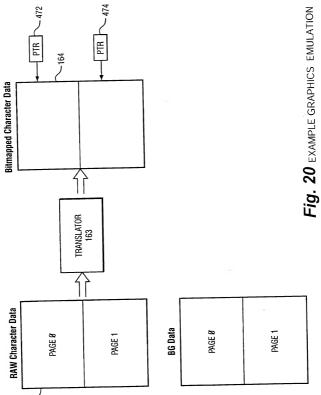
#### REGISTERS 0xFF00 P1 SB 0xFF01 SC 0xFF02 DIV 0xFF04 TIMA 0xFF05 TMA 0xFF06 0xFF07 TAC 0xFF0F ĪF 0xFF10 NR10 NR11 0xFF11 0xFF12 NR12 0xFF13 NR13 0xFF14 NR14 0xFF16 NR21 0xFF17 NR22 0xFF18 NR23 0xFF19 NR24 NR30 0xFF1A NR31 0xFF1B 0xFF1C NR32 0xFF1D NR33 0xFF1F NR34 0xFF20 NR41 0xFF21 NR42 0xFF22 **NR43** 0xFF23 NR44 0xFF24 NR50 NR51 0xFF25 0xFF26 NR52 LCDC 0xFF40 0xFF41 STAT 0xFF42 SCY 0xFF43 SCX LY 0xFF44 0xFF45 LYC 0xFF46 DMA BGP 0xFF47 OBP0 0xFF48 0xFF49 OBP1 WY 0xFF4A 0xFF4B WX 0xFF4D KEY1 0xFF4F VBK HDMA1 0xFF51 0xFF52 HDMA2 0xFF53 HDMA3 0xFF54 HDMA4 0xFF55 HDMA5 **BCPS** 0xFF68 **BCPD** 0xFF69 **OCPS** 0xFF6A 0xFF6B OCPD 0xFE70 SVBK 0xFFFF

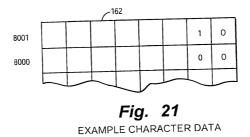
# Fig. 19B

EXAMPLE VIRTUAL
MICROPROCESSOR DATA STRUCTURES

-	,			
	Į	LCDC_BG		0X01
	ĺ	LCDC_OBJ	0x02	
		LCDC_OBJSIZE	0x04	
		LCDC_BGCODE		80x0
1		LCDC_BGCHR		0x10
		LCDC_WINDOW		0x20
		LCDC_WINCODE	0x40	
		LCDC_CONTROL	0x80	
	l			

1	STAT_MATCH		0X04
-	STAT_INT_HBLANK	0x08	
- {	STAT_INT_VBLANK	0x10	
	STAT_INT_OAM	0x20	
	STAT_INT_MATCH	0x40	





_164			Ī
0 0 0 0 0 0 0 0	8 × 8	8 × 8	PRE-RENDERED TILES (NOT COLORIZED)

Fig. 22

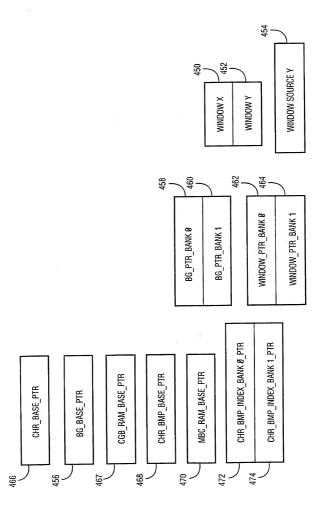


Fig. 23 EXAMPLE GRAPHICS OBJECT POINTERS

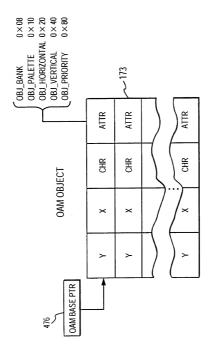
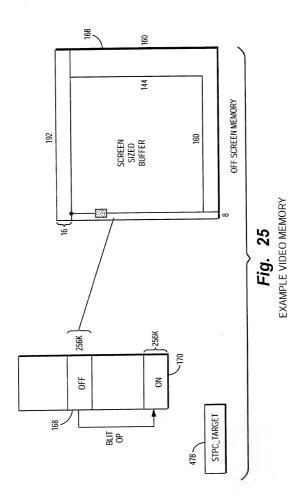


Fig. 24
EXAMPLE EMULATED OAM



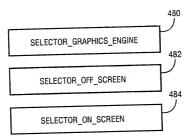


Fig. 26 EXAMPLE GRAPHICS MODE SELECTORS

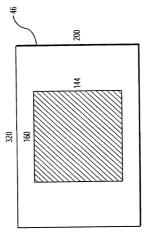


Fig. 27
EXAMPLE SCREEN LAYOUT

Fig. 28 EXAMPLE VGA MODE CONTROL

0x10
0x00
0x13
0x03
0x3C6
0x3C8
0x3C9
0x3DA
0x08

GE DESTINATION_BASE	0x018
GE_DESTINATION_PITCH	0x028
GE DESTINATION_XY	0x10000
GE HEIGHT	0x048
GE_PIXEL_DEPTH	0x07C
GE RASTER_OP	0x08C
GE_SOURCE_BASE	0x098
GE SOURCE_PITCH	0x0AC
GE SOURCE_XY	0x0BC
GE WIDTH	0xC8
<u> </u>	

Fig. 29 EXAMPLE GRAPHICS ENGINE REGISTER INDEXES